

## 5.0/3.3V PCMCIA SRAM RECHARGE CARDS

### Brief Description

The **CardPro™ *International*** range of 8/16bit SRAM Recharge Cards are alternatives to many similar Cards originally supplied by Centennial/Smart Modular, Whites EDC, Simpletech and others.

These SRAM Recharge Cards have been designed and are manufactured in England by **CardPro™ *International*** to stringent ISO9001-2008 technical and quality standards and are particularly suitable for PCMCIA compliant Industrial and Military applications.

Packaged in type I ultrasonically welded stainless steel housing

Memory sizes range from 512KB to 16MB with 45ns access time.

A key feature is the ability to operate on 3.3V and 5.0V DC supplies with dynamic performance unaffected down to 2.0V. This allows for possible host battery supply discharge conditions in portable equipment.

Back-up battery life between charges is enhanced by a unique charging circuit and the use of a high capacity battery

All Cards in the range will function over the Industrial temperature range of -40°C to +85°C.

Attribute memory and data protection switch are options. Standard Attribute Memory is 2KB Page write EEPROM. Byte write EEPROM and Byte write FRAM devices are options.

Cards are normally despatched with CardPro labelling, but custom labelling is a very low cost option.

Custom programming of Common and Attribute Memories are no cost options.

Resin Gel encapsulation is a cost option. This provides a PCB conformal coating to protect against moisture ingress and vibration damping to enable continuous operation in high vibration environments such as military helicopters.

### Features

- High performance PCMCIA SRAM Recharge Card
- Ultrasonically welded stainless steel housing
- Fast access time of 45ns
- 8/16bit PCMCIA standard interface
- Very low power CMOS technology
- Rechargeable environmentally friendly Manganese Dioxide Lithium data back-up battery with proven 10 year minimum useful life
- In built back-up battery charging circuit
- Attribute Memory optional. Standard uses 2KB Page write EEPROM. Byte write EEPROM or Byte write FRAM are available to special order.
- Attribute Memory data: CIS, FF or custom, no charge options
- Common Memory programming, no charge option
- Custom Labelling, low cost, no minimum order requirement option
- Resin Gel encapsulation, minimum order requirement cost option
- 2 year conditional warranty
- Fully RoHS compliant
- CE Declaration of Conformity

# Technical Specification

# CardPro™ International

Spec No: SRI16 Series – Ver 1.2 – 09.09

## Card Pin Connections

Pin	Signal Name	I/O	Function
1	GND	DC	Ground
2	D3	I/O	Data bit 3
3	D4	I/O	Data bit 4
4	D5	I/O	Data bit 5
5	D6	I/O	Data bit 6
6	D7	I/O	Data bit 7
7	CE1	I	Card Enable 1
8	A10	I	Address bit 10
9	OE	I	Output Enable
10	A11	I	Address bit 11
11	A9	I	Address bit 9
12	A8	I	Address bit 8
13	A13	I	Address bit 13
14	A14	I	Address bit 14
15	WE	I	Write Enable
16	Ready/Busy	N/A	N.C.
17	Vcc	DC	Supply Voltage
18	Vpp1	N/A	N.C.
19	A16	I	Address bit 16
20	A15	I	Address bit 15
21	A12	I	Address bit 12
22	A7	I	Address bit 7
23	A6	I	Address bit 6
24	A5	I	Address bit 5
25	A4	I	Address bit 4
26	A3	I	Address bit 3
27	A2	I	Address bit 2
28	A1	I	Address bit 1
29	A0	I	Address bit 0
30	D0	I/O	Data bit 0
31	D1	I/O	Data bit 1
32	D2	I/O	Data bit 2
33	WP	O	Write Protect
34	GND	DC	Ground

Pin	Signal Name	I/O	Function
35	GND	DC	Ground
36	CD1	O	Card Detect 1
37	D11	I/O	Data bit 11
38	D12	I/O	Data bit 12
39	D13	I/O	Data bit 13
40	D14	I/O	Data bit 14
41	D15	I/O	Data bit 15
42	CE2	I	Card Enable 2
43	VS1	O	Voltage Sense 1
44	N.C.		
45	N.C.		
46	A17	I	Address bit 17
47	A18	I	Address bit 18
48	A19	I	Address bit 19
49	A20	I	Address bit 20
50	A21	I	Address bit 21
51	Vcc	DC	Supply Voltage
52	Vpp2	N/A	N.C.
53	A22	I	Address bit 22
54	A23	I	Address bit 23
55	A24	I	Address bit 24
56	A25	I	Address bit 25
57	VS2	O	Voltage Sense 2
58	N.C.		
59	Wait	N/A	N.C.
60	N.C.		
61	REG	I	Attrib Mem Sel
62	BVD2	O	Batt V Detect 2
63	BVD1	O	Batt V Detect 2
64	D8	I/O	Data bit 8
65	D9	I/O	Data bit 9
66	D10	I/O	Data bit 10
67	CD2	O	Card Detect 2
68	GND	DC	Ground

### Notes:

CD1 and CD2 are grounded within the Card.

BVD1 is pulled up with 10K internal resistor.

CE1, CE2, OE, WE and REG are active low.

WP is active high.

VS1 is optionally grounded to indicate 3.3V/5V

## CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A0 - A25	INPUT	<b>ADDRESS INPUTS:</b> A0 through A25 enable direct addressing of up to 64MB of memory. A0 is not used in 16bit mode. A25 is the most significant bit.
DO - D15	INPUT/OUTPUT	<b>DATA INPUT/OUTPUT:</b> D0 through D15 constitute the bi-directional databus. D0 – D7 constitute the lower (even) Byte and D8 – D15 the upper (odd) Byte. D15 is the most significant Byte.
$\overline{CE1}$ , $\overline{CE2}$	INPUT	<b>CARD ENABLE 1 AND 2:</b> $\overline{CE1}$ enables even Byte accesses, $\overline{CE2}$ enables odd Byte accesses. Multiplexing A0, $\overline{CE1}$ and $\overline{CE2}$ allows 8bit hosts to access all data on D0 -D7.
$\overline{OE}$	INPUT	<b>OUTPUT ENABLE:</b> Active low signal enabling read data from the memory card.
$\overline{WE}$	INPUT	<b>WRITE ENABLE:</b> Active low signal enabling write data to the memory card.
$\overline{CD1}$ , $\overline{CD2}$	OUTPUT	<b>CARD DETECT 1 and 2:</b> Provide card insertion detection. These signals are connected to ground internally. Host systems must provide 10K ohm pull up resistors on these pins.
$\overline{WP}$	OUTPUT	<b>WRITE PROTECT:</b> When hardware WP switch is ON, signal is pulled high via 10K ohm resistor. When switch is off, signal is pulled down to ground.
Vcc	INPUT	<b>CARD POWER SUPPLY:</b> 5.0/3.3V for internal circuits, automatically selected within card.
GND		<b>GROUND:</b> Signal ground and power supply negative return.
$\overline{REG}$	INPUT	<b>ATTRIBUTE MEMORY SELECT:</b> Active high signal to select attribute memory.
BVD1, BVD2	OUTPUT	<b>BATTERY VOLTAGE DETECT:</b> Provides status of data back-up battery voltage. BVD2 = BVD1 = VoH, battery voltage guaranteed to retain data BVD2 = VoL, BVD1 = VoH, data valid, battery recharge desirable BVD1 = BVD2 =VoL, data valid, but battery requires immediate extended recharge to ensure data integrity.
$\overline{VS1}$ , $\overline{VS2}$	OUTPUT	<b>VOLTAGE SENSE:</b> Indicates host socket of card VCC requirement. VS1 = VS2 = OPEN = 5.0V only card. VS1= ground, VS2 = OPEN = 5.0/3.3V card. (All cards operate satisfactorily over the voltage range 6.0 to 2.0V, this voltage sense setting is optional)
N/A		<b>FUNCTION NOT APPLICABLE FOR SRAM CARDS</b>
N.C.		<b>NO INTERNAL CONNECTION TO CARD:</b> Pin may be driven or left floating

### Common Memory Read Function Truth Table

Function Mode	REG	CE2	CE1	A0	OE	WE	D[15::8]	D[7::0]
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8bits)	H	H	L	L	L	H	High-Z	Even-Byte
	H	H	L	H	L	H	High-Z	Odd-Byte
Word Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Odd Byte Only Access	H	L	H	X	L	H	Odd-Byte	High-Z

### Common Memory Write Function Truth Table

Function Mode	REG	CE2	CE1	A0	OE	WE	D[15::8]	D[7::0]
Standby Mode	X	H	H	X	X	X	X	X
Byte Access (8 bits)	H	H	L	L	H	L	X	Even-Byte
	H	H	L	H	H	L	X	Odd-Byte
Word Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Only Access	H	L	H	X	H	L	Odd-Byte	X

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Spec no: SRI16 Series - Ver 1.2– 09.09

**Attribute Memory Read Function Truth Table**

Function Mode	REG	CE2	CE1	A0	OE	WE	D[15::8]	D[7::0]
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8 bit)	L	H	L	L	L	H	High-Z	Even-Byte
	L	H	L	H	L	H	High-Z	Not Valid
Word Access (16bit)	L	L	L	X	L	H	Not Valid	Even-Byte
Odd Byte Only Access	L	L	H	X	L	H	Not Valid	High-Z

**Attribute Memory Write Function Truth Table**

Function Mode	REG	CE2	CE1	A0	OE	WE	D[15::8]	D[7::0]
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8 bit)	L	H	L	L	H	L	X	Even-Byte
	L	H	L	H	H	L	X	X
Word Access (16 bit)	L	L	L	X	H	L	X	Even-Byte
Odd Byte Only Access	L	L	H	X	H	L	X	X

## DC Characteristics

Symbol	Parameter	Density	Min	Typical	Max	Units	Test Conditions
ICC	Vcc Active Current	256KB to 16MB	3	3.5	5	mA	VCC = 5.25V tcycle = 45ns
ICCS	VCC Standby Current	All	0.7	1.25	2	mA	VCC = 5.25V Control Signals = VCC
ILI	Input Leakage Current	All			±20	µA	VCC = VCCMAX Vin = VCC or VSS
ILO	Output Leakage Current	All			±20	µA	VCC = VCCMAX Vin = VCC or VSS
VIL	Input Low Voltage	All	0		0.5	V	
VIH	Input High Voltage	All	3		VCC +0.5	V	
VOL	Output Low Voltage	All			0.4	V	IOL = 3.2mA
VOH	Output High Voltage	All	VCC- 0.4		VCC	VCC	IOH = 2.0mA

### Notes:

CMOS Test Conditions: VIL = VSS ± 0.2V, VIH = 5.0V ± 0.2V. T = 25°C

All Currents are RMS Values

Control Signals:  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$ ,  $\overline{REG}$ .

ICCS includes 3.0V data back-up battery recharge current which depends on battery discharge level. ICCS min is specified for fully charged battery. ICCS typical value is specified for battery discharged to approximately 2.7V. ICCS Max is specified for battery discharged to 1.0V

Values are the same for all memory densities

### Absolute Maximum Values:

Operating Temperature: -40°C to +85°C

Storage Temperature: -60°C to +95°C

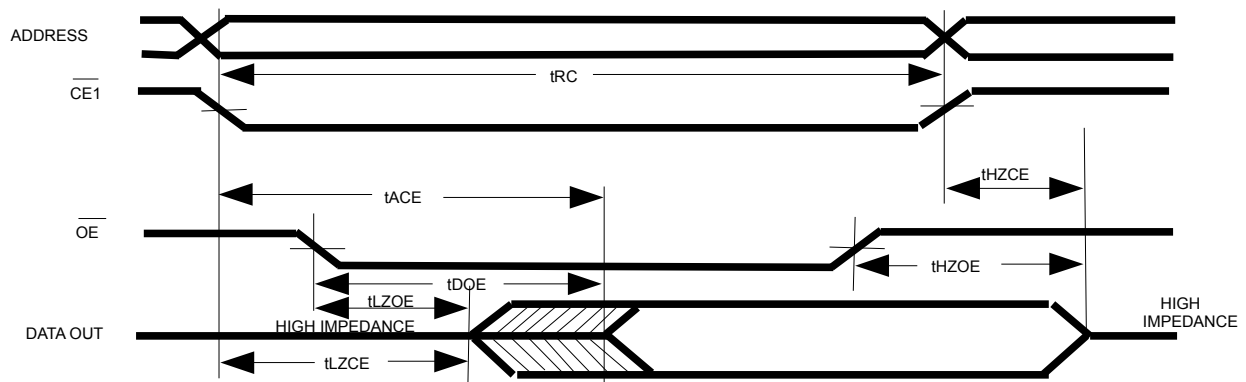
Voltage on any pin relative to VSS -0.5V to +5.5V During transitions, inputs may undershoot to -2.0V or overshoot to VCC +2.0V for periods less than 20ns

VCC supply voltage relative to VSS -0.5V to +7.0V

**AC Characteristics**

**Read Cycle**

Parameter	Description	Min	Max	Unit
$t_{RC}$	Read Cycle Time	45		ns
$t_{AA}$	Address to Data Valid		45	ns
$t_{OHA}$	Data Hold from Address Change	10		ns
$t_{ACE}$	$\overline{CE1}$ or $\overline{CE2}$ LOW to Data Valid		45	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z		18	ns
$t_{LZCE}$	$\overline{CE1}$ or $\overline{CE2}$ LOW to Low Z	10		ns
$t_{HZCE}$	$\overline{CE1}$ or $\overline{CE2}$ HIGH to High Z		18	ns
$t_{PU}$	$\overline{CE1}$ or $\overline{CE2}$ LOW to Power Up	0		ns
$t_{PD}$	$\overline{CE1}$ or $\overline{CE2}$ HIGH to Power Down		45	ns

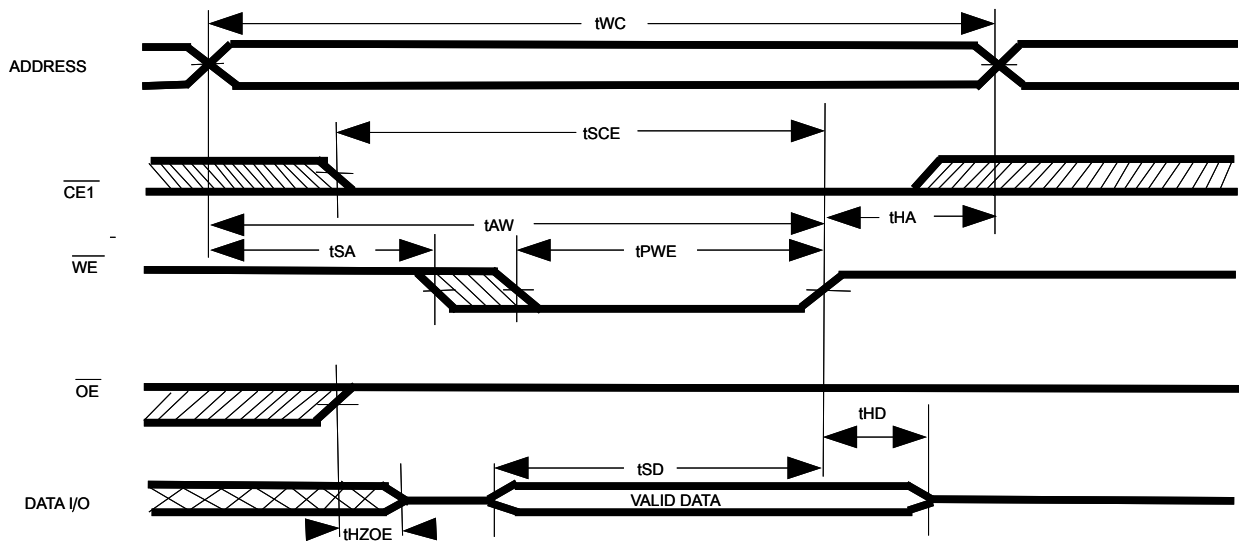


**Read Cycle Timings**

AC Characteristics

Write Cycle

Parameter	Description	Min	Max	Unit
$t_{WC}$	Write Cycle Time	45		ns
$t_{SCE}$	$\overline{CE1}$ or $\overline{CE2}$ LOW to Write End	35		ns
$t_{AW}$	Address setup to Write End	35		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Setup to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		ns
$t_{SD}$	Data Setup to Write End	25		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z		18	ns
$t_{LZWE}$	$\overline{WE}$ LOW to High Z	10		ns



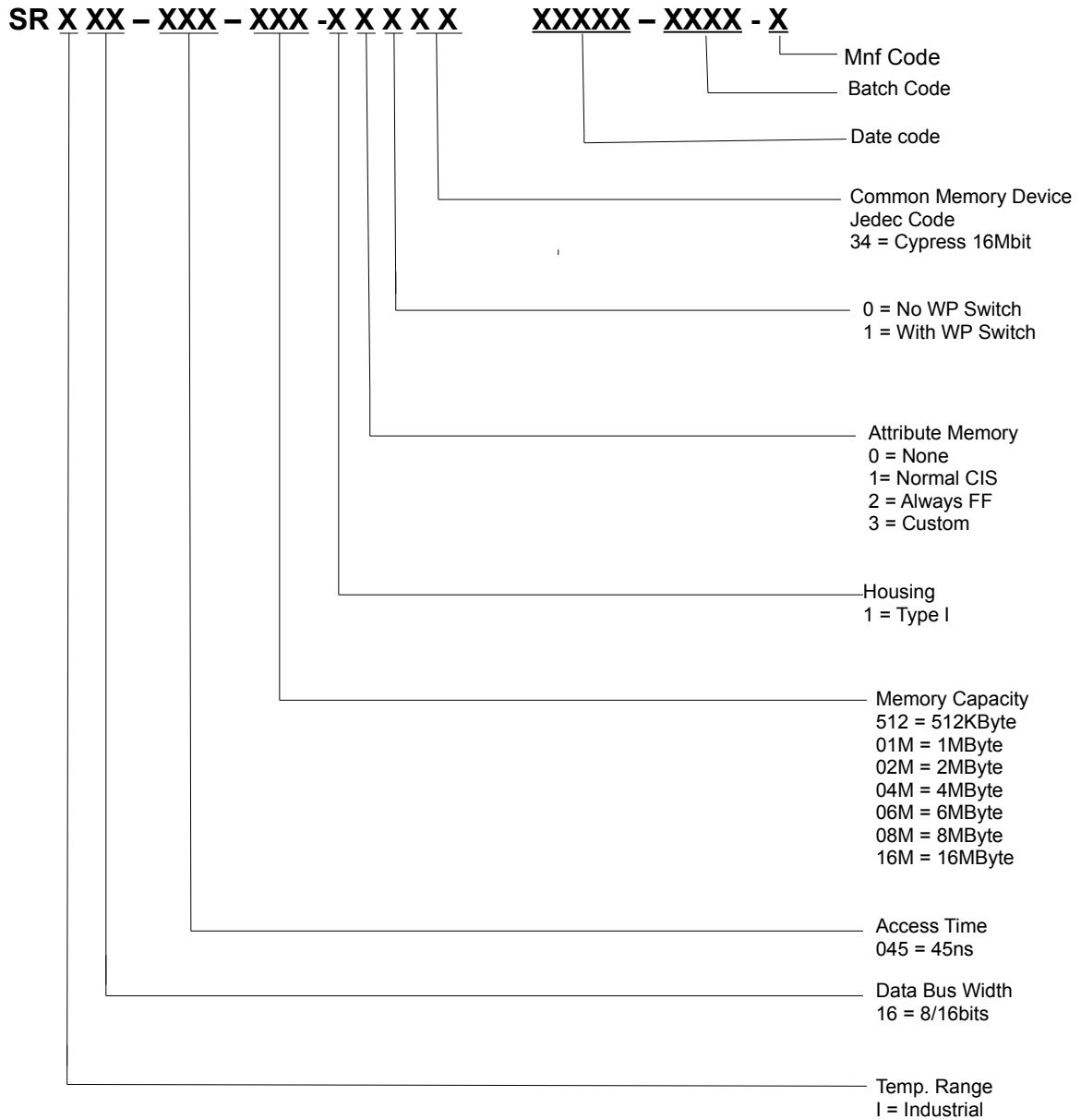
Write Cycle Timings

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# CardPro™ International

## SRAM Card Part Number Information



Card Professionals Limited – Trading as

**CardPro™ International**

Sandhurst House  
297 Yorktown Road  
Sandhurst

Berkshire, GU47 0QA United Kingdom

Tel: +44(0)1276 609777 Fax: +44 (0)1276 609888

Email: [sales@cardprointernational.com](mailto:sales@cardprointernational.com) Web: [www.cardprointernational.com](http://www.cardprointernational.com)

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